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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CHEN, CHIA WEI A	

ART UNIT	PAPER NUMBER
2622	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/761,319	RHODES ET AL.	
	Examiner	Art Unit	
	Chia-Wei A. Chen	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *70-79 and 120-130* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *70-79 and 120-130* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/22/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The references listed on the Information Disclosure Statement filed on 1/22/2004 have been considered by the examiner (see attached PTO/SB/08).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 70 and 120 and 123 are rejected under 35 U.S.C. 102(e) as being anticipated by Clark et al. (US 5,859,450).

As to claim 70, Clark et al. teaches, in Figure 6, an imager comprising:

- a CMOS imager (Fig. 1) comprising an array of pixel sensor cells formed in a retrograde well on a substrate, wherein each pixel sensor cell has a photosensitive region, a photosensor formed on the photosensitive region, and a floating diffusion region for receiving and outputting image charge received from the photosensitive region (col. 2, lines 54-58; col. 4, lines 13-20), and
- a circuit (Fig. 6) formed in the substrate and electrically connected to the array for receiving and processing signals representing an image output by the array and for

providing output data representing the image (output to image capture system; col. 5, lines 20-23); and

- a processor (609) for receiving and processing data representing the image (col. 5, lines 13-16).

As to claim 120, Clark et al. teaches, in Figure 6, a CMOS imager comprising:

- an array of pixel sensor cells formed in a retrograde well in a substrate, each of said pixel sensor cells being separated by an isolation region that electrically isolates said pixel cells from each other (col. 2, lines 54-58; col. 4, lines 13-20), and each said pixel sensor cell comprising:
- a photoconversion device (602);
- a reset transistor (614);
- a source follower transistor (616);
- a row select transistor (622); and
- a floating diffusion region (618) in electrical communication with said photoconversion device and said source follower transistor (col. 5, lines 8-30).

As to claim 123, Clark et al. teaches the CMOS imager of claim 120 wherein the photoconversion device is a photodiode (col. 2, lines 50-51).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 71-79 and 125-130 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clark '450 in view of Burr (US 6,093,951).

As to claim 71, Clark et al. teaches the imager of claim 70, but does not teach wherein said CMOS imager and said processor are formed on a single substrate.

Burr teaches wherein said CMOS imager and said processor are formed on a single substrate (the above processes are performed at many locations on a single substrate so that multiple MOS devices are formed simultaneously to produce an integrated circuit; col. 16, lines 17-19).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the single chip of Burr with the imager of Clark et al. in order to reduce the conduction path resistance. (See col. 3, lines 40-44 of Burr.)

As to claim 72, Burr discloses substantially the claimed invention as set forth in the discussion for claim 72. Burr does not disclose expressly wherein the CMOS imager is formed on a first substrate, and said processor is formed on a second substrate.
As the time of the invention, it would have been obvious to a person of ordinary skill in the art to configure wherein the CMOS imager is formed on a first substrate, and said processor is formed on a second substrate. Applicant has not disclosed that configuring the processor to be formed on a second substrate provides an advantage, is used for a particular purpose

or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with either the CMOS imager and processor formed on a single substrate taught by Burr or wherein the claimed CMOS imager is formed on a first substrate, and said processor is formed on a second substrate because both designs perform the same function of capturing and processing an image. Therefore, it would have been obvious to modify Burr to obtain the invention as specified in claim 72.

As to claim 73, Clark et al. teaches the imager of claim 70, Burr teaches wherein the retrograde well has a dopant concentration within the range of about 1×10^{16} to about 2×10^{18} atoms per cm^3 at the bottom of the retrograde well (col. 8, lines 21-24 of Burr).

As to claim 74, Clark et al. in view of Burr teaches the imager of claim 73, Burr teaches wherein the retrograde well has a dopant concentration within the range of about 5×10^{14} to about 1×10^{17} atoms per cm^3 at the top of the retrograde well (col. 8, lines 18-21 of Burr).

As to claim 75, Clark et al. teaches the imager of claim 70, Burr teaches wherein the retrograde well has a dopant concentration within the range of about 5×10^{16} to about 1×10^{18} atoms per cm^3 at the bottom of the retrograde well (col. 8, lines 21-24 of Burr).

As to claim 76, Clark et al. in view of Burr teaches the imager of claim 75, Burr teaches wherein the retrograde well has a dopant concentration within the range of about 1×10^{15} to 5×10^{16} atoms per cm^3 at the top of the retrograde well (col. 8, lines 18-21 of Burr).

As to claim 77, Clark et al. teaches the imager of claim 70, Burr teaches wherein the retrograde well has a dopant concentration of about 3×10^{17} atoms per cm^3 at the bottom of the retrograde well (col. 8, lines 21-24 of Burr).

As to claim 78, Clark et al. in view of Burr teaches the imager of claim 77, wherein the retrograde well has a dopant concentration of about 5×10^{15} atoms per cm^3 at the top of the retrograde well (col. 8, lines 18-21 of Burr).

As to claim 79, Clark et al. teaches the imager of claim 70, Burr wherein the retrograde well is a first retrograde well, and said circuit is formed in a second retrograde well (The CMOS retrograde well architecture taught by Burr may be used to construct the circuit disclosed by Clark et al.)

As to claim 125, Clark et al. teaches the CMOS imager of claim 120, Burr teaches wherein said retrograde well is provided to reflect signal carriers back to the photoconversion device (mobile charge carriers experience less mobility degradation due to impurity scattering; col. 8, lines 26-29 of Burr).

As to claim 126, Clark et al. teaches the CMOS imager of claim 120, Burr teaches wherein said retrograde well has a vertically graded dopant concentration (col. 8, lines 12-17 of Burr).

As to claim 127, Clark et al. teaches the CMOS imager of claim 126, Burr teaches wherein said vertically graded dopant concentration of the retrograde well is lowest at a top of the well and highest at a bottom of the well (col. 8, lines 12-17 of Burr).

As to claim 128, Clark et al. in view of Burr teaches the CMOS imager of claim 127, wherein said vertically graded dopant concentration at the top of the retrograde well is within the range of about 5×10^{14} to 1×10^{17} atoms per cm^3 and the concentration at the bottom of the retrograde well is within the range of about 1×10^{16} to 2×10^{18} atoms per cm^3 (col. 8, lines 18-24 of Burr).

As to claim 129, Clark et al. in view of Burr teaches the CMOS imager of claim 127, wherein said vertically graded dopant concentration at the top of the retrograde well is within the range of about 1×10^{15} to 5×10^{16} atoms per cm^3 and the concentration at the bottom of the retrograde well is within the range of about 5×10^{16} to 1×10^{18} atoms per cm^3 (col. 8, lines 18-24 of Burr).

As to claim 130, Clark et al. in view of Burr teaches the CMOS imager of claim 127, wherein said vertically graded dopant concentration at the top of the retrograde well is about 5×10^{15} atoms per cm^3 and the concentration at the bottom of the retrograde well is about 3×10^{17} atoms per cm^3 (col. 8, lines 18-24 of Burr).

6. Claims 122 and 124 rejected under 35 U.S.C. 103(a) as being unpatentable over Clark et al. (US 5,859,450).

Clark et al. discloses substantially the claimed invention as set forth in the discussion for claims 122 and 124.

Clark et al. does not disclose expressly wherein the photoconversion device is a photogate or a photoconductor.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to configure the photoconversion device to be a photogate or a photoconductor. Applicant has not disclosed that configuring the photoconversion device to be a photogate or a photoconductor provides an advantage, is used for a particular purpose or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with either the photodiode taught by Clark et al. or the claimed photogate or photoconductor because both the photogate and photoconductor perform the same function of collecting electric charges based on incident light. Therefore, it would have been obvious to modify Clark et al. to obtain the invention as specified in claims 122 and 124.

7. Claim 121 is rejected under 35 U.S.C. 103(a) as being unpatentable over Clark et al. in view of Guidash (US 6,657,665 B1).

As to claim 121, Clark et al. teaches the imager of claim 120 but does not teach wherein the photoconversion device further comprises a transfer transistor positioned to gate charges between said photoconversion device to said floating diffusion region.

Guidash teaches, in Figure 4, wherein the photoconversion device further comprises a transfer transistor (transfer gates TG1a) positioned to gate charges between said photoconversion device to said floating diffusion region (col. 4, lines 30-53).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the transfer gates of Guidash in order to to provide an alternate pixel architecture that has a large fill factor, and the capability to perform CDS that also have more linear charge to voltage conversion. (See col. 2, lines 49-53 of Guidash.)

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Maegawa et al. (US 5,191,399) teaches a solid-state imaging device with improved photodetector.

Inquiries

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chia-Wei A. Chen whose telephone number is 571-270-1707. The examiner can normally be reached on Monday - Friday, 7:30 - 17:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, NgocYen Vu can be reached on (571) 272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

cac.
10/5/2007

NGOC-YEN VU
SUPERVISORY PATENT EXAMINER